Future of smart processing

Dynamic Architecture

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Chariot Technologies Lab., Inc.
919, North Market Street, Suite 950,
Wilmington, County of New Castle,
DE, Zip 19801
www.chariotlab.com

Global hunger for computing power

Unprecedented demand for computing resources provoked by the rise of AI vastly outpaces current supply capabilities

... WHILE TRADITIONAL CHIP TECHNOLOGIES
ARE REACHING PHYSICAL LIMITS

...AND QUANTUM COMPUTING
IS NOT READY YET

OpenAI Majors are rushing
Microsoft to develop own chips

NVIDIA. AI chips are reportedly sold out until 2025

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Processing should be SMART

High-performance dynamic processor capable to adjust its architecture to best fit the incoming sets of instructions - next logical step from static architectures

Dynamic processing techniques aim to minimize the number of clock cycles by accommodating maximum instructions per each clock cycle
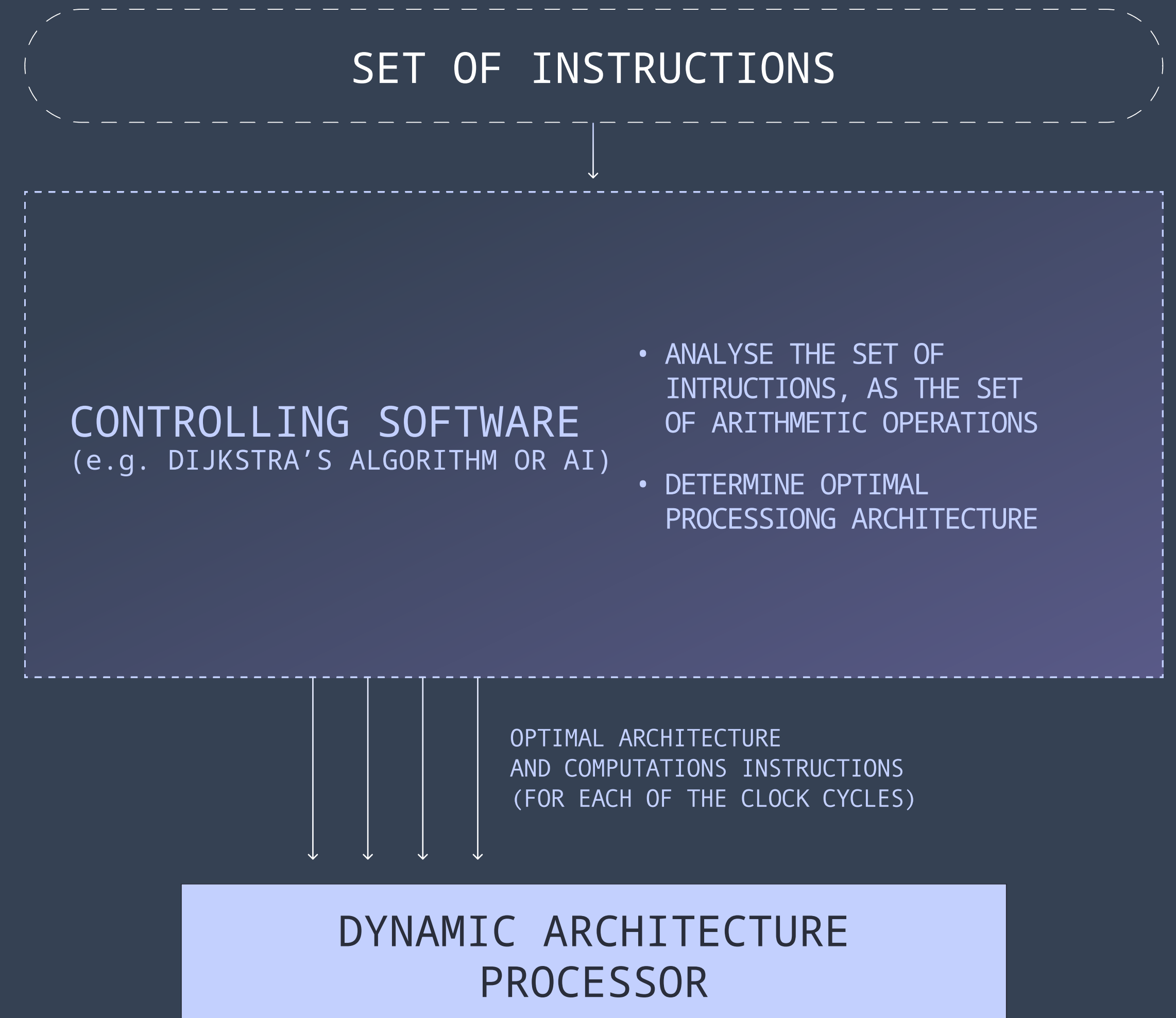
THE FIRST EVER 'UNIVERSAL ASIC'

MADE POSSIBLE WITH FIONa TECHNOLOGY

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Concept based on FIONa

FIONa transforms incoming instructions into math formulas and enables proper analysis to determine optimal architecture for each clock cycle

Dynamic processor receives 'optimal architecture with data to compute' instructions for each clock cycle

SET OF INSTRUCTIONS

CONTROLLING SOFTWARE
(e.g. DIJKSTRA'S ALGORITHM OR AI)

- ANALYSE THE SET OF INTRUCTIONS, AS THE SET OF ARITHMETIC OPERATIONS

- DETERMINE OPTIMAL PROCESSIONG ARCHITECTURE

OPTIMAL ARCHITECTURE
AND COMPUTATIONS INSTRUCTIONS
(FOR EACH OF THE CLOCK CYCLES)

DYNAMIC ARCHITECTURE PROCESSOR

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Prototype testing results

First dynamic architecture processor was prototyped on FPGA PYNQ-Z1 from Xilinx

Same algorithm (16-128 RISC instructions randomly generated by ChatGPT) was executed on two devices

FPGA over M2 Max of MacBook Pro results –
4x fewer cycles and 3x less execution time

DESPITE:

- INITIAL PYNQ-Z1 MUCH LOWER CAPACITY
- NON-OPTIMAL FPGA PROGRAMMABLE BLOCKS
- LOSSES ON LAN COMMUNICATION

```
Downloads — -zsh — 76×33
[(base) timurryspekov@Timurs-MacBook-Pro downloads % python test.py
asm file:file.asm
21
M2 Max: 4
Fiona: 1
Dif 3.39
[(base) timurryspekov@Timurs-MacBook-Pro downloads % python test.py
asm file:file.asm
41
M2 Max: 7
Fiona: 2
Dif 3.36
[(base) timurryspekov@Timurs-MacBook-Pro downloads % python test.py
asm file:file.asm
82
M2 Max: 12
Fiona: 3
Dif 3.68
[(base) timurryspekov@Timurs-MacBook-Pro downloads % python test.py
asm file:file.asm
164
M2 Max: 22
Fiona: 6
Dif 3.17
(base) timurryspekov@Timurs-MacBook-Pro downloads %
```

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Why now the time?

The Moore's Law is coming to an end while demand for high-performance computing was never that high as:

- TECHNOLOGICAL REVOLUTION CONTINUES
- AI JUST STARTS ITS INCONCEIVABLE JOURNEY
- CHIP WARS ARE GAINING MOMENTUM

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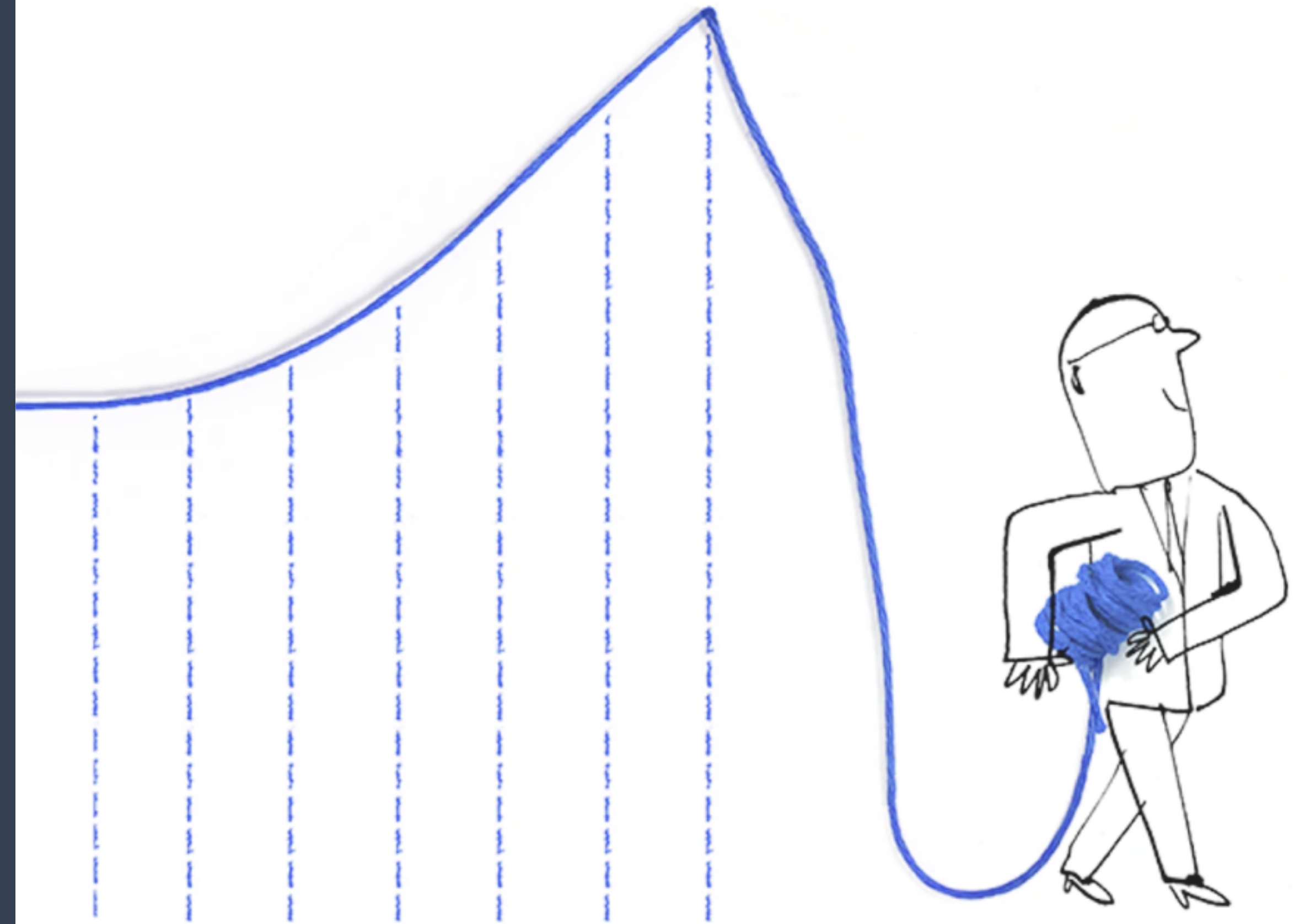
A trillion dollar industry by 2030

We can target most of the verticals of global semiconductors industry due to:

- SURPASSING PERFORMANCE OF THE CONCEPT
- ITS ENERGY EFFICIENCY, AND
- UNIVERSAL APPLICATION

Areas to benefit the most include AI, robotics, IoT, personal computers, mobile devices

Only AI chip market is expected to reach $400 bln. by 2027

McKinsey & Co.

The overall growth in the global semiconductor market is driven by the automotive, data storage, and wireless industries.

Global semiconductor market value by vertical, indicative, $ billion

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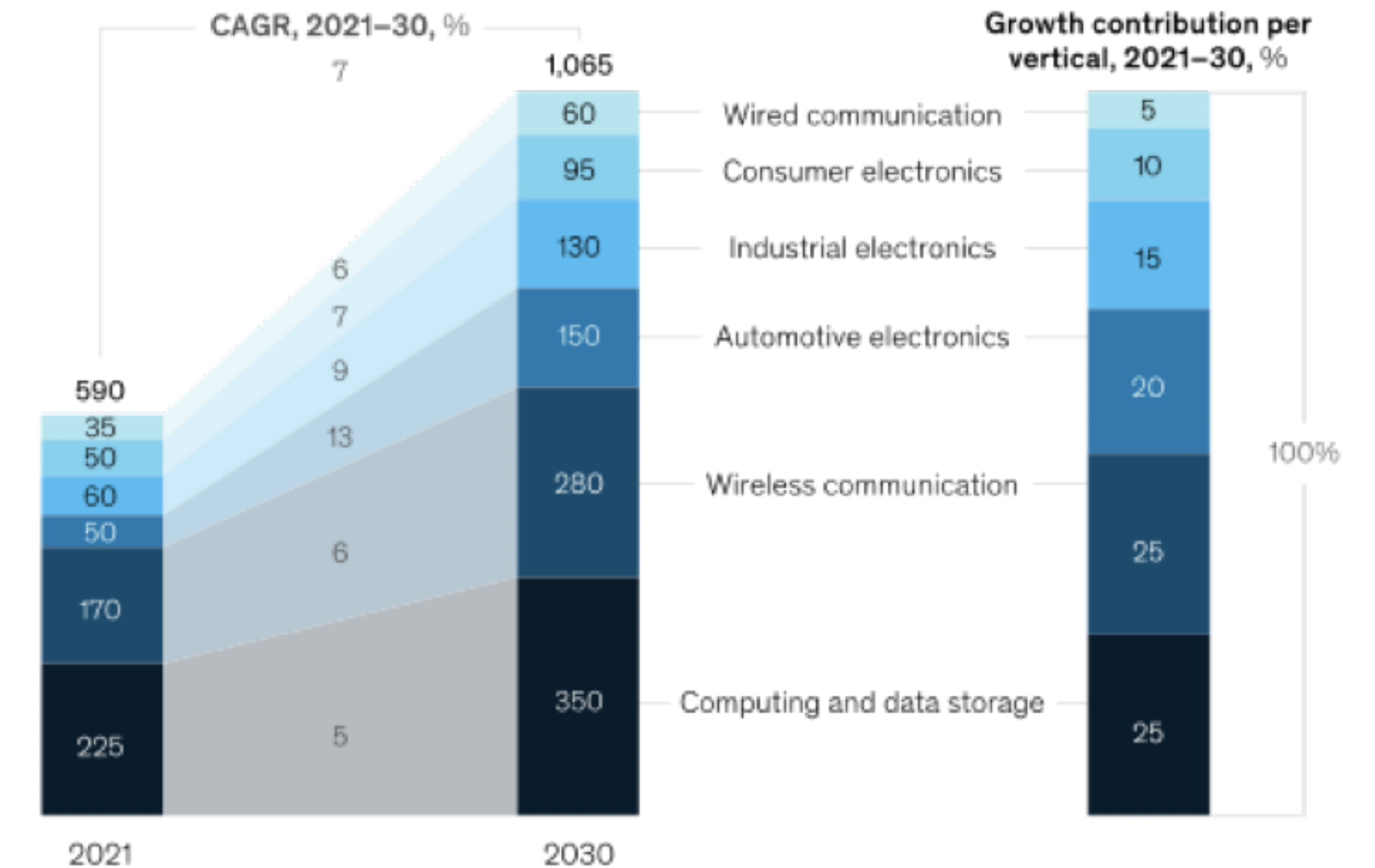
Competition matters less for inventors

With IP rights protected in major jurisdictions we mostly beware of potential infringers than healthy competition

Prior art search proved that real dynamic processing (on a clock cycle level) existed for a long time as a perspective concept only without any real implementation so far

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Achieved milestones

FIRST PATENT
ISSUED IN USA

PATENT ISSUED
IN TAIWAN

FIRST FIONA-POWERED RISC-V
PROCESSOR SIMULATED/TESTED ON
MAKERCHIP PLATFORM

PATENT PENDING IN
SEVERAL OTHER
JURISDICTIONS

FIRST DYNAMIC
ARCHITECTURE PROTOTYPED/
TESTED ON FPGA

JUN'21	APR'22	DEC'22	AUG'23	OCT'23	JAN'24	FEB'24

SEP'22	OCT'23	DEC'23

PCT
APPLICATION
PUBLISHED

PATENT ISSUED
IN JAPAN

PATENT
ALLOWED
IN EUROPE

DYNAMIC
PROCESSING CONCEPT
R&D STARTED

PATENT APPLICATION
ON DYNAMIC
PROCESSING FILED

FIONa technology
(conversion of conditional statements into math)

Dynamic processing
architecture

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